In the Claims:

1. (Currently Amended) A method for modulating a fractional-N synthesizer (F-N synthesizer) ~~F-N synthesizer~~ in response to applied sequences of in-phase (I) and quadrature (Q) analog modulation signals, said F-N synthesizer comprising a loop divider having a variable fractional divisor, the method comprising:

comparing said sequence of I analog modulation signals with a first plurality of threshold values at successive time intervals, thereby to generate a sequence of I digital output signals, said sequence of I digital output signals corresponding to respective relationships between said sequence of I analog modulation signals and said plurality of ~~thresholds~~ first threshold values at said successive time intervals[[,]];

comparing said sequence of Q analog modulation signals with a second plurality of threshold values at successive time intervals, thereby to generate a sequence of Q digital output signals, said sequence of Q digital output signals corresponding to respective relationships between said sequence of Q analog modulation signals and said plurality of ~~thresholds~~ second threshold values at said successive time intervals[[,]];

transforming said sequences of I and Q digital output signals into a sequence of digital modulation signals in accordance with a predetermined relationship between values of said I and Q digital output signals in consecutive time intervals[[,]]; and

modifying said variable fractional divisor in accordance with said sequence of digital modulation signals.

2. (Currently Amended) The method of claim ~~1wherein~~ 1 wherein:

said first plurality of threshold values comprises a threshold value equal to a predetermined function of a maximum absolute value of positive peak values for said sequence of I analog modulation signals and a threshold value equal to a predetermined function of a maximum absolute value of negative peak values for said sequence of I analog modulation signals[[,]]; and

said second plurality of threshold values comprises a threshold value equal to a predetermined function of a maximum absolute value of positive peak values for said sequence of Q analog modulation signals and a threshold value equal to a predetermined function of a

maximum absolute value of negative peak values for said sequence of Q analog modulation signals.

3. (Currently Amended) The method of claim 2 wherein:

said first plurality of threshold values comprises a value substantially equal to 0.7 times the positive peak value of said sequence of I analog modulation signals, and a value substantially equal to 0.7 times the negative peak value of said sequence of I analog modulation signals[[,]]; and

said second plurality of threshold values comprises a value substantially equal to 0.7 times the positive peak value of said sequence of Q analog modulation signals, and a value substantially equal to 0.7 times the negative peak value of said sequence of Q analog modulation signals.

4. (Currently Amended) The method of claim 1 wherein:

said sequence of I digital output signals ~~comprise~~ comprises at least three values[[,]];

said sequence of Q digital output signals ~~comprise~~ comprises at least three values[[,]]; and

wherein said predetermined relationship between values of said sequence of I digital output signals and said sequence of Q digital output signals in consecutive time intervals comprises a predetermined relationship between said sequences of I and Q digital output signals in two consecutive time intervals.

5. (Currently Amended) The method of claim 4 wherein said sequences of I and Q analog modulation signals are GMSK modulation signals.

6. (Currently Amended) The method of claim 5 wherein

said at least three values for said sequence of I digital output ~~values~~ signals and said at least three values for said sequence of Q digital output ~~values~~ signals are each represented as +1, 0, and -1[[,]]; and ~~wherein~~

wherein for states N and N+1 corresponding to values for said sequence of I digital output ~~values~~ signals and said sequence of Q digital output ~~values~~ signals in respective consecutive time intervals N and N+1, said sequence of digital modulation signals are given by:

State N	State N+1	Digital Modulation Signal
I=0,Q=1	I=1,Q=0	-1
I=0,Q=1	I=-1,Q=0	+1
I=1,Q=0	I=0,Q=-1	-1
I=1,Q=0	I=0,Q=1	+1
I=0,Q=-1	I=-1,Q=0	-1
I=0,Q=-1	I=1,Q=0	+1
I=-1,Q=0	I=0,Q=1	-1
I=-1,Q=0	I=0,Q=-1	+1.

7-8. (Canceled).

9. (Currently Amended) ~~The method of claim 8~~ In a radio transmitter having a fractional-N synthesizer (F-N synthesizer) comprising a loop divider having a variable fractional divisor, a method for generating digital modulation signals in response to input analog modulation signals comprising:

comparing said analog modulation signals at a plurality of successive time intervals with at least one predetermined threshold value to derive a sequence of digital values;

decoding said sequence of digital values to generate a corresponding sequence of digital modulation signals; and

modifying said variable fractional divisor in accordance with said digital modulation signals,

wherein said at least one predetermined threshold value comprises at least one value equal to a predetermined function of a peak value of said analog modulation signals, ~~wherein~~ said at least one value equal to a predetermined function of a peak value comprises one positive threshold value equal to a predetermined percentage of a positive peak value of said analog modulation signals and one negative threshold value equal to a predetermined percentage of a negative peak value of said analog modulation signals.

10. (Currently Amended) The method of claim 9 wherein:

a first of said digital values, represented as +1, is achieved when said analog modulation signals ~~exceeds~~ exceed said positive threshold value at a predetermined time[[,]];

a second of said digital values, represented as a -1, is achieved when said analog modulation signals are more negative than said negative threshold value at said predetermined time[[,]]; and

a third of said digital values, represented as a 0, is achieved when neither of said first or second digital values is achieved.

11. (Currently Amended) ~~The method of claim 7 wherein~~ In a radio transmitter having a fractional-N synthesizer (F-N synthesizer) comprising a loop divider having a variable fractional divisor, a method for generating digital modulation signals in response to input analog modulation signals comprising:

comparing said analog modulation signals at a plurality of successive time intervals with at least one predetermined threshold value to derive a sequence of digital values;

decoding said sequence of digital values to generate a corresponding sequence of digital modulation signals; and

modifying said variable fractional divisor in accordance with said digital modulation signals;

said analog modulation signals comprise in-phase (I) analog modulation signals and quadrature (Q) analog modulation signals[[,]]; and

said comparing comprises comparing said I analog modulation signals and said Q analog modulation signals separately with respective predetermined threshold values to derive separate sequences of digital values corresponding to ~~each said~~ each of said I and Q analog modulation signals.

12. (Currently Amended) The method of claim 11 wherein said decoding comprises decoding said separate sequences of digital values corresponding to each of said I and Q analog modulation signals to generate said digital modulation signals.

13. (Canceled).

14. (Currently Amended) ~~The converter of claim 13~~ A signal converter comprising:

an input circuit for receiving analog modulation signals;

at least one comparator for comparing at least one of said analog modulation signals with at least one threshold signal level to produce a first output digital signal when said at least one analog modulation signal bears a first relationship to said at least one threshold signal level, and to produce a second output digital signal when said at least one analog modulation signal bears a second relationship to said at least one threshold signal level;

a decoder for receiving said first and second output digital signals from said at least one comparator and outputting digital modulation signals corresponding to said analog modulation signals; and

a divider circuit having a variable fractional divisor determined by said digital modulation signals,

wherein said analog modulation signals comprise in-phase (I) analog modulation signals and quadrature (Q) analog modulation signals.

15. (Original) The converter of claim 14 wherein said analog modulation signals comprise GMSK analog modulation signals.

16. (Currently Amended) The converter of claim 14 wherein said at least one threshold signal level comprises two threshold ~~signals~~ signal levels, a first of which comprises a function of a most positive value of said analog modulation signals, and a second of which comprises a function of a most negative value of said analog modulation signals.

17. (Currently Amended) The converter of claim 16 wherein said at least one comparator comprises comparators for comparing each of said ~~I and Q~~ analog modulation signals with each of said first and second threshold ~~signals~~ signal levels.

18. (Currently Amended) The converter of claim 17 wherein said comparators provide first output digital signals and second output digital signals corresponding to each of said ~~I and Q~~ analog ~~input~~ modulation signals.

19. (Currently Amended) The converter of claim 18 wherein said decoder receives said first and second output digital signals corresponding to each of said ~~I and Q~~ analog ~~input~~ modulation signals and outputs digital modulation signals corresponding to both of said ~~I and Q~~ ~~input~~ analog modulation signals.

20. (Canceled).

21. (Currently Amended) ~~The converter of claim 20 further comprising~~ A signal converter comprising:

an input circuit for receiving analog modulation signals;

at least one comparator for comparing at least one of said analog modulation signals with at least one threshold signal level to produce a first output digital signal when said at least one analog modulation signal bears a first relationship to said at least one threshold signal level and to produce a second output digital signal when said at least one analog modulation signal bears a second relationship to said at least one threshold signal level;

a decoder for receiving said first and second output digital signals from said at least one comparator and outputting digital modulation signals corresponding to said analog modulation signals;

a divider circuit having a variable fractional divisor determined by said digital modulation signals, wherein said divider circuit is a loop divider in a fractional-N (F-N) synthesizer; and

a switch for applying digital modulation signals from said decoder to said divider circuit.

22. (Currently Amended) ~~The converter of claim 20 further comprising~~ A signal converter comprising:

an input circuit for receiving analog modulation signals;

at least one comparator for comparing at least one of said analog modulation signals with at least one threshold signal level to produce a first output digital signal when said at least one analog modulation signal bears a first relationship to said at least one threshold signal level and to produce a second output digital signal when said at least one analog modulation signal bears a second relationship to said at least one threshold signal level;

a decoder for receiving said first and second output digital signals from said at least one comparator and outputting digital modulation signals corresponding to said analog modulation signals;

a divider circuit having a variable fractional divisor determined by said digital modulation signals, wherein said divider circuit is a loop divider in a fractional-N (F-N) synthesizer; and

a switch for applying digital modulation signals to said divider circuit from a source other than said decoder.

23. (Currently Amended) ~~The converter of claim 20 further comprising~~ A signal converter comprising:

an input circuit for receiving analog modulation signals;

at least one comparator for comparing at least one of said analog modulation signals with at least one threshold signal level to produce a first output digital signal when said at least one analog modulation signal bears a first relationship to said at least one threshold signal level and to produce a second output digital signal when said at least one analog modulation signal bears a second relationship to said at least one threshold signal level;

a decoder for receiving said first and second output digital signals from said at least one comparator and outputting digital modulation signals corresponding to said analog modulation signals;

a divider circuit having a variable fractional divisor determined by said digital modulation signals, wherein said divider circuit is a loop divider in a fractional-N (F-N) synthesizer; and

a switch operating based on at least one control signal for applying digital modulation signals from:

said decoder to said divider circuit in response to a first state of said at least one control signal ~~a first set of control signals,~~; and

a source other than said decoder to said divider circuit in response to a second state of said at least one control signal ~~a second set of control signals,~~; and ~~wherein~~

wherein said first and second states of said at least one control signal ~~sets of control signals~~ are mutually exclusive.